Electronic Version

Stylesheet Version v1.1.1

[INTEGRATED CIRCUIT YIELD ENHANCEMENT USING VORONOI DIAGRAMS]

Abstract

A method of calculating critical area in an integrated circuit design, said method comprising: inputting an integrated circuit design; associating variables with the positions of edges in said integrated circuit design; and associating cost functions of said variables with spacing between said edges in said integrated circuit design; wherein said cost functions calculate critical area contributions as the positions and length of said edges in said integrated circuit design change, and wherein said critical area contributions comprise a measure of electrical fault characteristics of said spacing between said edges in said integrated circuit design.